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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/157,655	09/21/98	DIERICKX	B	IMEC88.00CP1

MM92/0705

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EXAMINER	
LUU,T	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 07/05/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/157,655	DIERICKX, BART	
	Examiner	Art Unit	
	Thanh X Luu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *15 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. Applicant's election without traverse of Claims 13-15 in Paper No. 11 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by the publication of Ricquier et al ("Pixel Structure with Logarithmic Response for Intelligent and Flexible Imager Architectures", 1992).

Regarding claim 13, Ricquier et al disclose (see Figure 2) a pixel for imaging applications fabricated in MOS technology, the pixel comprising: a photosensitive element and a first transistor (M1) having a gate and a first and second electrode and being in series with the photosensitive element, the first transistor and the photosensitive element forming a first connection; a second transistor (M3) having a gate, the second transistor being coupled to the first connection forming a second connection, the second transistor being part of an amplifying circuit; and a third

transistor (M2) having a gate and having two electrodes, the third transistor being connected in the second connection between the first connection and the second transistor.

4. Claims 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by the publication of Aw et al ("A 128 X 128-Pixel Standard-CMOS Image Sensor with Electronic Shutter", December 1996).

Regarding claim 13, Aw et al disclose (see Figure 3) a pixel for imaging applications fabricated in MOS technology, the pixel comprising: a photosensitive element and a first transistor (M4) having a gate and a first and second electrode and being in series with the photosensitive element, the first transistor and the photosensitive element forming a first connection (pd); a second transistor (M1) having a gate, the second transistor being coupled to the first connection forming a second connection, the second transistor being part of an amplifying circuit; and a third transistor (M3) having a gate and having two electrodes, the third transistor being connected in the second connection between the first connection and the second transistor.

Regarding claim 14, Aw et al disclose (see Figure 3) the gate of the first transistor (M4) is at a first voltage (Reset) and the first electrode of the first transistor is at a second voltage (Vreset), the second electrode of the first transistor being connected to the photosensitive element, the gate of the second transistor (M1) being connected to the third transistor (M3).

Regarding claim 15, Aw et al disclose (see Figure 3) the gate of the first transistor is at a first voltage and wherein one of the electrodes of the third transistor is connect to the gate of the second transistor and the other of the electrodes is connected to the first connection (pd).

5. Claims 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Buhler et al (U.S. Patent 5,742,047).

Regarding claim 13, Buhler et al disclose (see Figure 1) a pixel for imaging applications fabricated in MOS technology, the pixel comprising: a photosensitive element (D1) and a first transistor (M1) having a gate and a first and second electrode and being in series with the photosensitive element, the first transistor and the photosensitive element forming a first connection (10); a second transistor (M4) having a gate, the second transistor being coupled to the first connection forming a second connection, the second transistor being part of an amplifying circuit; and a third transistor (M2) having a gate and having two electrodes, the third transistor being connected in the second connection between the first connection and the second transistor.

Regarding claim 14, Buhler et al disclose (see Figure 1) the gate of the first transistor (M1) is at a first voltage and the first electrode of the first transistor is at a second voltage, the second electrode of the first transistor being connected to the photosensitive element, the gate of the second transistor (M4) being connected to the third transistor (M2).

Regarding claim 15, Buhler et al disclose (see Figure 1) the gate of the first transistor is at a first voltage and wherein one of the electrodes of the third transistor is connect to the gate of the second transistor and the other of the electrodes is connected to the first connection (10).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X. Luu whose telephone number is (703) 305-0539. The examiner can normally be reached on Monday-Friday from 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seungsook Ham, can be reached on (703) 308-4090. The fax phone number for the organization where the application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

txl

June 27, 2000

Que T. Le
Primary Examiner